REMARKS

The present Amendment amends claims 1 and 18 and leaves claims 2-8, 11, 12, 17 and 19-29 unchanged. Therefore, the present application has pending claims 1-8, 11, 12 and 17-29.

The Examiner is respectfully requested to contact Applicants' Attorney, the undersigned, by telephone so as to schedule an interview so as to discuss the outstanding issues of the present application prior to examination.

In the Office Action, the Examiner again rejected claims 1, 5, 8, 11, 17, 18, 22, 23, 26 and 27 under 35 USC §103(a) as being unpatentable over Tanabe (U.S. Patent No. 5,752,272) in view of Johnson (U.S. Patent No. 5,761,137); rejected claims 2, 19 and 20 under 35 USC §103(a) as being unpatentable Tanabe, Johnson in view of Genduso (U.S. Patent No. 5,778,422); rejected claims 3, 4 and 21 under 35 USC §103(a) as being unpatentable over Tanabe, Johnson and Conary (U.S. Patent No. 5,935,253); rejected claims 12 and 18 under 35 USC §103(a) as being unpatentable over Tanabe, Johnson, Genduso and Handy (book entitled: "The Cache Memory Book"); and rejected claims 6 and 24 under 35 USC §103(a) as being unpatentable over Tanabe, Johnson and Suzuki (U.S. Patent No. 5,381,532). These rejections are traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in the claims are not taught or suggested by Tanabe, Johnson, Genduso, Conary, Handy and Suzuki whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections.

Amendments were made to independent claims 1 and 18 so as to more clearly describe features of the present invention. Particularly, amendments were made to these claims to more clearly recite that the present invention is directed to a structure for prefetching data from a memory to a processor wherein a first bus is provided for the transfer of an instruction code from the memory to the processor to be executed by the processor and a second bus is provided for the transfer of operand data from the memory to the processor to be processed by the processor during execution of instruction codes. These features of the present invention allows for the independent transfer to the processor of operand data while, for example, an instruction code is prefetched. Thus, for example, the present invention can efficiently transfer instruction codes and operand data in parallel.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by any of the references of record, particularly Tanabe, Johnson, Genduso, Conary, Handy and Suzuki whether taken individually or in combination with each other.

In the Office Action the Examiner readily admits that:

> "Tanabe does not explicitly disclose at least two memory buses connecting the memory controller and the memory, the at least two memory buses comprising a first memory bus for transferring an instruction code and a second memory bus for transferring operand data."

The Examiner recognizing the above noted deficiencies of Tanabe attempts to supply these deficiencies by combining Tanabe with Johnson. In the Office Action the Examiner alleges that:

> "Johnson teaches the concept of two memory buses comprising a first memory bus for transferring an instruction code (Fig. 1, reference 16) and a second bus for transferring operand data [data] (Fig. 1, reference 20). This feature taught by Johnson provides a means for simultaneously transferring control information and data".

Further in the Office Action, the Examiner responding to the arguments presented in the Remarks of the February 2, 2004 Amendment, states with respect to said arguments that:

> "as noted by the Applicants, the first bus taught by Johnson transfers instruction information on the bus. This instruction information is submitted as bits, which is a code and thus the instruction information is an instruction code".

It appears from the above that the Examiner has completely missed the point of the arguments presented in the Remarks of the February 2, 2004 Amendment and attributed an allegation to Applicants which was never stated by Applicants nor was it Applicants intention to make such statement if the record seems to supply such. To the extent that such arguments require clarification the following is provided.

Johnson merely discloses the conventional structure of a processor 12 being connected to a memory 22 by a memory controller 14. The processor 12 is connected to the memory controller 14 by a control bus 16, an address bus 18 and a data bus 20. In Johnson, the control bus 16 supplies control signals to the memory controller 14 so as to control the operation of the memory controller 14. These control signals are primarily intended for the processor 12 to control the memory controller 14 and for the memory controller 14 to provide status type signals to the processor 12 so as to indicate the state of operation of the memory controller 14.

There is no teaching or suggestion in Johnson that the control signals that may exist on the control bus 16 are codes which have been retrieved from the memory 22. Nor is there any teaching or suggestion in Johnson that the control signals which may exist on the control bus 16 are in fact instruction codes to be executed by the processor 12. The control signals taught by Johnson are simply control signals which are output by the processor 12 onto control bus 16 so as to control the operation of the memory controller 14 and as such are not signals which have been retrieved from the memory 22 so as to be executed by the processor 12 as in the present invention.

Thus, since Tanabe as admitted by the Examiner does not teach or suggest two different buses, wherein a first bus transfer an instruction code to be executed by the processor and the second bus transfers operand data to be processed by the processor during execution of instruction codes, and Johnson suffers from the very same deficiencies, it is quite clear that the combination of Tanabe and Johnson fails to teach or suggest the features of the present invention as recited in the claims. Therefore, reconsideration and withdrawal of the 35 USC §103(a) rejection of claims 1, 5, 8, 11, 17, 18, 22, 23, 26 and 27 as being unpatentable over Tanabe and Johnson is respectfully requested.

The above noted deficiencies of Tanabe and Johnson are not supplied any of the other references of record. Particularly, the above described features shown above not to be taught or suggested by Tanabe or Johnson are also not taught or suggested by Genduso, Conary, Handy and Suzuki. Thus, combining Tanabe and Johnson with one or more of Genduso, Conary, Handy and Suzuki would still fail to

teach or suggest the features of the present invention as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the other rejections of the claims under 35 USC §103(a) based on the combinations of Tanabe and Johnson with one or more of Genduso, Conary, Handy and Suzuki is respectfully requested.

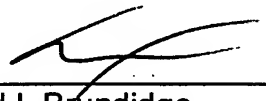
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-8, 11, 12 and 17-29.

In view of the foregoing amendments and remarks, Applicants submit that claims 1-8, 11, 12 and 17-29 are in condition for allowance. Accordingly, early allowance of claims 1-8, 11, 12 and 17-29 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.36683CX1).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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